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Evaluation of hardware costs of implementing PSK signal detection circuit based on "system on chip"

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Abstract. The article deals with the choice of the architecture of digital signal processing units for implementing the PSK signal detection scheme. As an assessment of the effectiveness of architectures, the required number of shift registers and computational processes are used when implementing the "system on a chip" on the chip. A statistical estimation of the normalized code sequence offset in the signal synchronization scheme for various hardware block architectures is used.

1. Introduction

The hardware architecture of the digital signal processing units is one of the priority areas in improving the consumer qualities of digital transmitting devices and reducing their cost. The constant growth in the volume of transmitted digital information is accompanied by an increase in the requirements for the quality of communication. The increase in the density of the computing units of microcircuits per unit volume allows satisfying the growing requirements due to the use of more complex pipeline algorithms for digital signal processing while maintaining the power consumption of microcircuits.

Reception of the band signal begins with the synchronization of the code sequence of the receiver. After synchronization, the signal passes through the code detector [1]. The detection of the signal is carried out by means of consistent filtering according to the known code sequence. Usually, the sampling frequency of the signal is selected from four Nyquist frequencies and higher. A higher sampling frequency directly affects either the frequency of the digital receiver operation or the hardware costs of implementing the detector.

The digital signal detection circuit of the PSK type modulation is shown in 'figure 1' and consists of the following digital blocks: CORDIC-based harmonic signal generator; frequency conversion unit; synchronization code sequence generator; code synchronization unit; detector code sequence generator; detection unit by symbol table.



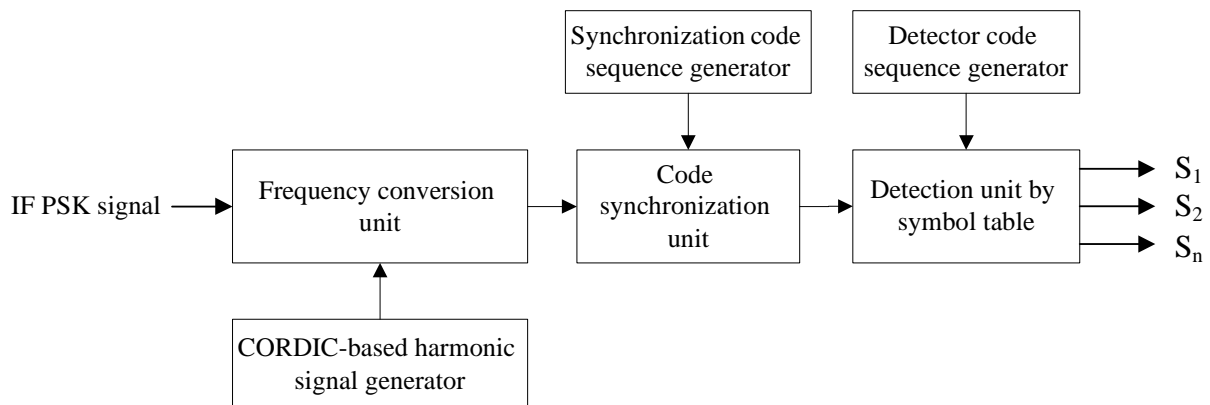


Figure 1. PSK signal detection circuit.

2. Overview of hardware architectures of signal processing units

All of the above-mentioned blocks of digital signal processing can be implemented through summation and logical shift operations. Therefore, to evaluate the hardware costs of implementing architectures, one can perform a comparative analysis of different architectures of adders and evaluate the statistical characteristics of the tracking signal at the output of the signal tracking unit.

2.1. Adder architecture

The simplest architecture in implementation is that with sequential bitwise summation of binary numbers [2, 3]. The base computational element of this architecture is called the full adder (FA). The total adder contains the inputs: the transfer signal, the summand signals and the outputs: the transfer signal, the sum signal. The delay in calculating the sum for this architecture depends on the composition of the bit sequences. The maximum delay in the calculation depends linearly on the length of the terms, since at each iteration it is necessary to take into account the propagation of the carry bit.

More efficient architecture in computing speed is that with pre-computing of the carry bit [2]. In this architecture, the carry generation and the carry propagation bits are calculated. Based on the values of the carry generation and the carry propagation bits, a pre-computing of the carry bit is performed for a group of bits at once, which proportionally reduces the calculation time of the sum. The delay in calculating the sum in this architecture also depends on the composition of the bit sequence of the terms. But unlike the architecture with sequential calculation of the carry bit, the maximum time for calculating the sum depends on the length of the terms and on the length of the pre-calculation block of the carry bits.

Another effective architecture is based on the pre-calculation of the sum of the bit group for the two input values of the carry bit. The true value of the sum of the bit group is selected based on the calculated carry bit value. The difference between this architecture and the architecture with the pre-calculation of the carry bit is that the group is summed serially. The maximum delay in computing this architecture depends on the length of the terms and on the length of the pre-calculation block of the carry bit.

Another kind of adder architecture depends on the probability that a group of bits will appear with the generation or propagation of the carry bit. Calculation of the amount for such a group of bits can be omitted. This architecture combines the advantages of the adder architecture with the pre-calculation of the carry bit and the architecture with the selection of the carry bit. The maximum delay in calculating the sum of the bit sequences depends on the length and composition of the bit group.

The computational delays of the above-described architectures are given in table 1.

Table 1.Delays in calculating the sum of two 14-bit numbers.

Architecture:	Min. delay, clock cycles	Max. delay, clock cycles
Ripple-Carry adder	3	15
Carry-Lookahead adder	2	4
Carry-Select adder	4	5
Carry-Skip adder	4	15

2.2. Frequency Conversion Unit

The frequency conversion block is realized on the basis of complex multiplication of the information signal at the intermediate frequency and the local oscillator signal. The complex multiplier is realized on the basis of the above described adder architectures. Pipeline computation is used to minimize the computation delay. As a result, the delay in computing the product corresponds to the delay of the adder with the chosen architecture.

The number of required signals and processes for different architectures of the frequency conversion unit is given in table 2.

Table2.Necessary hardware resources for frequency conversion block.

Based on the following architecture:	Flip-flops	Processes
Ripple-Carry adder	31563	5175
Carry-Lookahead adder	37026	7419
Carry-Select adder	40971	8970
Carry-Skip adder	30045	6729

2.3. CORDIC-based harmonic signal generator

As a local oscillator, a harmonic signal generator with a continuous phase is used. [4,5]. The architecture of the generator is based on a CORDIC processor with dual pipelining. The hardware implementation of the local oscillator required 23404 shift registers and 1142 computational processes.

2.4. Synchronization code sequence generator and code synchronization unit

The signal synchronization unit is based on two correlators and a feedback loop. For the study, 28 bit correlators based on the above combiner architectures were developed. The number of required signals and processes for the implementation of the synchronization block is given in table 3.

Table3. Necessary hardware resources for synchronization block.

Based on the following architecture:	Flip-flops	Processes
Ripple-Carry adder	15030	2464
Carry-Lookahead adder	17632	3533
Carry-Select adder	19510	4271
Carry-Skip adder	14307	3204

To evaluate the statistical characteristics, a computer simulation of the synchronization circuit was carried out. Since the architectures of the adders have different computational delays, a different sampling frequency of the PSK signal was selected based on the data in table 1 at a fixed frequency of the chip operation [6]. The simulation results are shown in 'figure 2', 'figure 3', 'figure 4'.

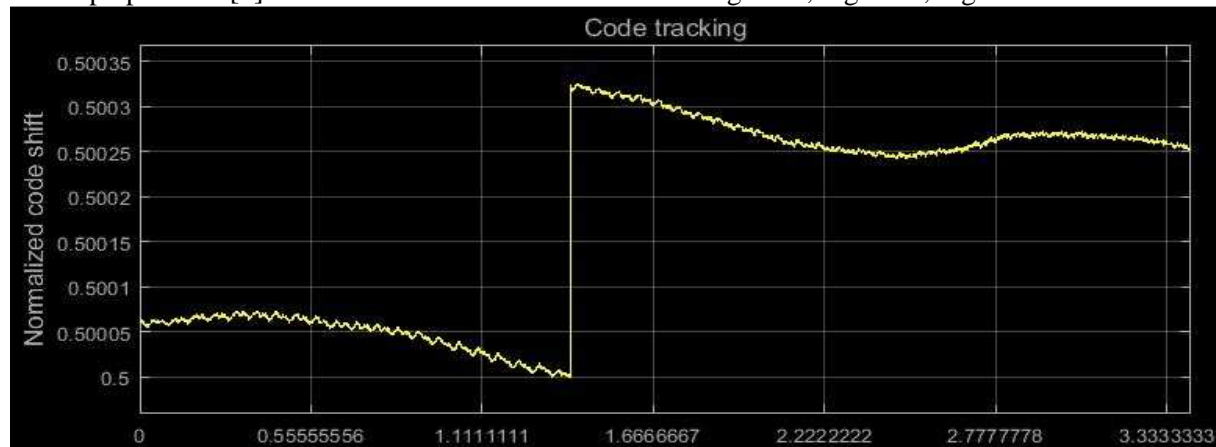


Figure 2. Scheme of synchronization of PSK signal by code sequence based on Ripple-Carry and Carry-Skip adder.



Figure 3. Scheme of synchronization of PSK signal by code sequence based on Carry-Select adder.



Figure 4. Scheme of synchronization of PSK signal by code sequence based on Carry-Lookahead adder.

As a statistical indicator of the synchronization scheme, the synchronization error and the standard deviation are used in table 4.

Table 4. Normalized code shift statistics.

Based on the following architecture:	Mean-square error	Standard deviation
Ripple-Carry and Carry-Skip adder	0.0009595	0.00005793
Carry-Select adder	0.000072	0.0001423
Carry-Lookahead adder	0.00009876	0.00009661

2.5. Detector code sequence generator and detection unit by symbol table

The hardware costs of the information symbol detector are linearly dependent on the dimension of the symbol table. A summary table of hardware costs is given in table 5, table 6.

Table 5. Necessary flip-flop registers for code detector.

Modulation type:	Ripple-Carry adder	Carry-Skip adder	Carry-Select adder	Carry-Lookahead adder
BPSK	3006	2861	3902	3526
QPSK	6012	5723	7804	7052
8PSK	12024	11446	15608	14105

Table 6. Necessary compute processes for code detector.

Modulation type:	Ripple-Carry adder	Carry-Skip adder	Carry-Select adder	Carry-Lookahead adder
BPSK	9600	8972	11960	9892
QPSK	13800	17944	23920	19784
8PSK	27600	35888	47840	39568

3. Conclusion

The above architectures were tested on the basis of the hardware and software National Instruments. The hardware implementation was written in the VHDL language for the Xilinx Kintex k410t chip and launched in the LabView FPGA using the NI FlexRIO PXIe-7976R board. The given data allow one to make a choice of the most suitable architecture of the digital detector, depending on the requirements for the frequency of operation of the chip, the amount of available hardware computational units and the conditions for receiving the PSK signal.

4. Acknowledgement

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References

- [1] B Sklar 2003 *Digital Communications Fundamentals and Applications* (Los Angeles: Prentice Hall PTR)
- [2] B Parhami 2012 *Algorithms and design methods for digital computer arithmetic* (New York: Oxford University Press)
- [3] A.V. Sokolovskiy, A.B. Gladyshev, D.D. Dmitriev and V.N.Ratushniak 2017 Hardware Diagram of Computing Devices of Navigation Equipment of Consumers SRNS. *2017 IEEE Dynamics of Systems, Mechanisms and Machines (Dynamics)* 1-4
- [4] A.V.Sokolovskii, D.D. Dmitriev, I.N.Kartsan, and A.E.Concharov 2018 A harmonic signal generator with c continuous phase. *2018 Moscow Workshop on Electronic and Networking*
- [5] E.C. Ifechor and B.W. 2002 Jervis *Digital Signal Processing. A Practical approach* (NJ: Prentice Hall)
- [6] Pereira de Lucena, Antonio Macilio; de Almeida Filho, Magno Prudencio; de Figueredo, Caio Gomes; Pimentel, Diego Braga; do Nascimento Rios, Clauson Sales; Tavares Ferreira da Silva, Francisco de Assis 2017 Fully digital BPSK demodulator for satellite suppressed carrier telecommand system. *Int. J. Satell. Commun. Network.* **4** 359-374